Things Intelligented by DEEPX

CEO Lokwon Kim

DEEPX

DEEPX MISSION | AI of Things

Ubiquitous AI

AI of Things

The era of AI will create new and diverse applications embedded in things.

DEEPX

Embedded AI Specialist

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DEEPX's Disruptive Innovation

Power Consumption
- 300W ~

Price Range
- $1,500
- $5,000
- $30,000

NVIDIA

Power Consumption
Est. 2W ~ 5W

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Price Range
Under $100

NVIDIA GPU vs. DEEPX NPU

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Disruptive Innovation | "IT'S REAL"

NVIDIA Model: Tesla V100 16GB

- Performance: 56TOPS
- Efficiency: 0.18TOPS/W
- Price: Approx. $3,000
- Power Consumption: 300W

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https://youtu.be/V3f8ZRe-KfY?t=58

DEEPX's Flagship Model : DX-M1

- Performance: 23TOPS
- Efficiency: 10TOPS/W
- **Price: Approx. $70**
- **Power Consumption: 3~5W**

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https://youtu.be/V3f8ZRe-KfY?t=58

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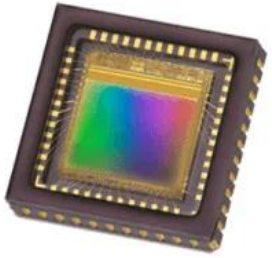
Extreme Case: Ultra Low Power NPU

Custom NPU Architecture

Intelligent CMOS Image Sensor

- **Face Detection Function NPU**
  - ✓ **Lower than 10mW**
  - ✓ **Always-on Function**



Always-on Smart CIS

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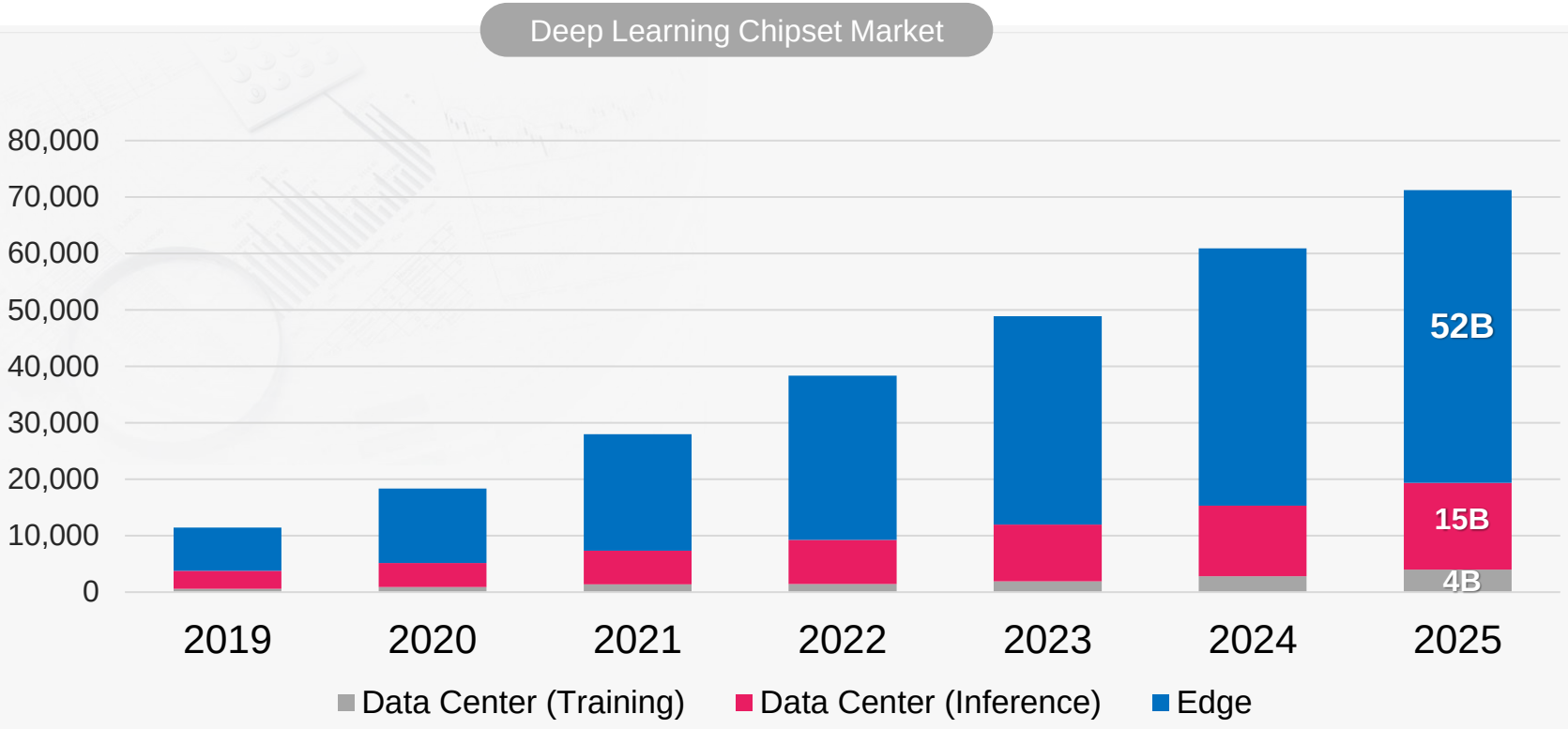
Market Overview

The AI Chipset market reached $11B in 2019 and reaching $71B by 2025.



Source : Omdia (前TRACTICA)

FOR DEEP LEARNING ACCELERATORS

DEEPX VISION | Super Intelligence Civilization

Leading Technological Advancement for Next Evolution

DEEPX

IP Strategy

✓ Patents

01 **More than 107+ Patents for NPU tech**

02 Constantly developing fundamentals of NPU

✓ Patent Portfolio

01 **Planning to file for more than 20 patents per year** (PCT, KR, US)

AI Applications	AI Memory Architecture	AI VISION/ISP	NPU	SoC	AR/VR Applications	Total
14	28	6	45	8	6	**107**

Business Model

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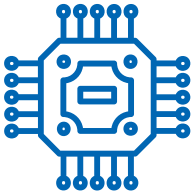
Business Area

01



SoC ASIC

Provide DEEPX NPU embedded commercial AI chips

02

Custom NPU IP Licensing

Provide one of the most efficient NPU design IPs for Strategical Partners

03

Custom SoC Design Service

Provide fully specialized custom SoC based on DEEPX NPU

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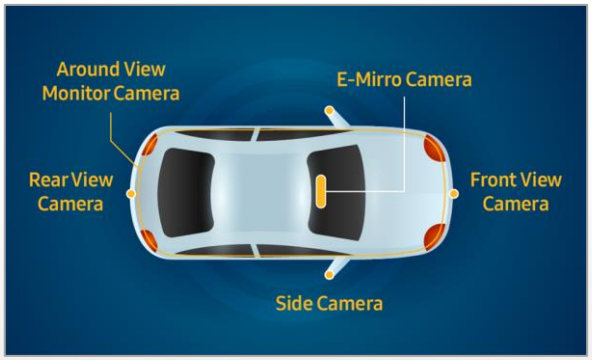
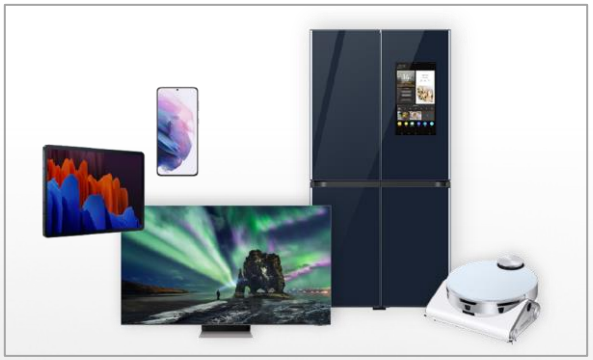
Target Market

Smart Camera Module

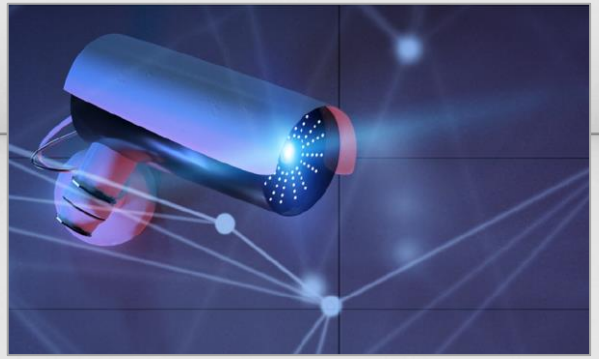
Automotive



Consumer Electronics



Surveillance System



Edge Computing

Smart Mobility / Drone

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Product Roadmap (2022)

01 DX-M1

- Performance: 23TOPS
- Efficiency: 10TOPS/W
- Core: ARM
- Process: 5nm
- Launching Date: 23.1Q

02 DX-H1

- Performance: Up to 22POPS
- Efficiency: 10TOPS/W
- Core: ARM
- Process: 5nm
- Launching Date: 23. 2Q

* DX H1C: PCIe Card (368TOPS)
* DX H1S: DX H1C x 10ea (3.7POPS)
* DX H1R: DX H1S x 6ea (22POPS)

03 DX-L1

- Performance: 2.4TOPS
- Core: RISC-V
- Process: 28nm
- Launching Date: 23.1Q

04 DX-L2

- Performance: 6.4TOPS
- Core: RISC-V
- Process: 14nm
- Launching Date: 22.4Q

** TOPS: Tera Operation Per Second ** POPS: Peta Operation Per Second

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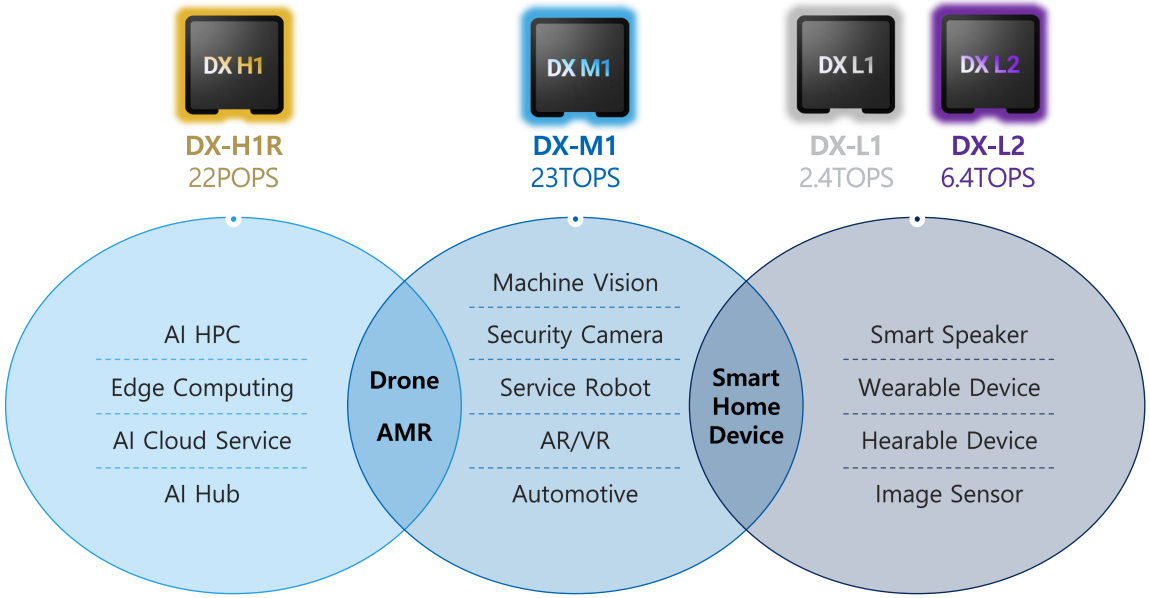
Business & Product Portfolio

DX-H Series

DX-M Series

DX-L Series



DEEPX Supply Chain Management

1 Work tools	2 Design IP	3 Back-End Design	4 Foundry	5 Package
cadence	ARM	GAON CHIPS	SAMSUNG	Amkor Technology
SYNOPSYS	CEVA	ASICLAND	tsmc	HANA MICRON
XILINX	SYNOPSYS	socionext		

DEEPX Blitz-Scaling Strategy

Toward the most customer centric company

01 Investors **(Series A&B $25Mil)**

CAPSTONE SHINHAN BANK KDB

02 NPU developments

- Preparing the first NPU chip fabrication in 2022
- **Demonstrated the first version of basic NPU (mid 2019)**

03 Achievements

- **100+ Patents** for NPU technology
- Government funds for NPU technology (ca.$30Mil)

04 International Business

- Established a branch in Silicon Valley (2018.8)

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Founder

Background

2007	· KETI (Alternative Military Service)
2007 - 2011	· Ph.D. in EE at UCLA
2008 - 2009	· Broadcom (Intern)
2010	· IBM T.J. Watson Research (Visiting)
2011 - 2014	· Cisco Systems
2014 - 2017	· Apple

Research Achievement

01 · 100+ Patents

02 · 10+ IEEE/ACM transactions journal paper (including Nature Astronomy)

Pioneer in NPU since 2010

ACM Transactions on
Reconfigurable Technology and Systems (TRETS)

A Fully Pipelined FPGA Architecture of a Factored Restricted Boltzmann Machine Artificial Neural Network

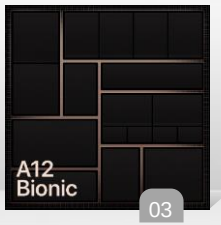
LOK-WON KIM, Cisco Systems
SAMEH ASAAD and RALPH LINSKER, IBM T. J. Watson Research Center

are present across multiple types of input. We obtain (in simulation) a 100-fold acceleration (vs. CPU software) for an fRBM having N = 256 units in each of its four groups (two input, one output, one intermediate group of units) running on a Virtex-6 LX760 FPGA. Many of the architectural features we implement are applicable not only to fRBMs, but to basic RBMs and other ANN algorithms more broadly.

Developed the world first edge NPU

01

02



03

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Man Power

J.W. KIM | Head of R&D

- **Former Project Director at Samsung Electronics**
- Georgia Tech PhD in Electrical Engineering
- Samsung: GPU development ; DSP development & commercialization

T.H. Kwon | Head of Business

- **Former US Branch President at COASIA**
- Samsung LSI ASIC Sales +20 years (US/EU)
- A wealth of experience in Global Sales & Marketing

NPU IP LEAD

NPU IP Design
20+ years

SNU · GCT · LG Electronics

MS at SNU

SoC TECH LEAD

SoC Chip Design
16+ years

INU 인천대학교 · LG Electronics

MS at Incheon Univ.

NPU TECH Jr

Energy-efficient PIM Architecture

KAIST

MS at KAIST

SW TECH LEAD

SW Framework
10+ years

SAMSUNG ELECTRONICS · UCLA

PhD at UCLA

RTL TECH LEAD

HW Processor Design
13+ years

세종대학교 SEJONG UNIVERSITY · dp

MS at Sejong Univ.

SW TECH LEAD

NPU Compiler
13+ years

AhnLab · KOREA UNIVERSITY

MS at Korea Univ.

Sys. SW LEAD

System Software
10+ years

Mando 만도 · LG Electronics

Experienced in Automotive Solutions

HRM & HRD

Human Resources
17+ years

SAMSUNG ELECTRONICS · SNU

MBA at SNU

Strategic Patents

Strategic Patents
13+ years

University of Strathclyde · LG Display

MS at Strathclyde

Strategic Marketing

Global Marketing
8+ years

SAMSUNG · SAMSUNG ELECTRO-MECHANICS · ILLINOIS

TECH MBA at UIUC