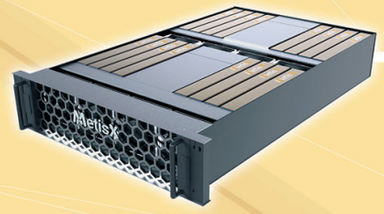
Leading the Data-Centric Computing World

The name “Metis” is derived from
the ancient Greek goddess of wisdom,
the letter “X” stands for acceleration,
emphasizing our mission to accelerate data centers
by embedding wisdom directly into memory.

Product Lineup–MetisX Computational Memory Series

CXL Computational Memory

MetisX CXL Computational Memory accelerates cache coherent large-scale data processing based on 1000s MetisX optimized cores, caches, and memory subsystem using a SW-defined approach.

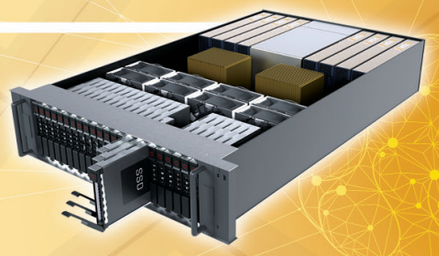


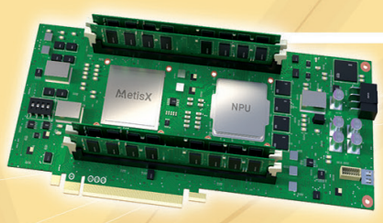
CXL Computational Memory Pool

MetisX CXL Computational Memory Pool accelerates large-scale data processing and drastically reduces data movement, which mitigates the long latency effect of far memory.

CXL Petabytes-Scale Infinite Memory Pool

MetisX CXL Petabytes-Scale Infinite Memory Pool based on SSD expansion enables the implementation of disaggregated memory system acceleration through sophisticated workload management in terms of latency/capacity tiering, thin provisioning, workload isolation, and nonvolatility.



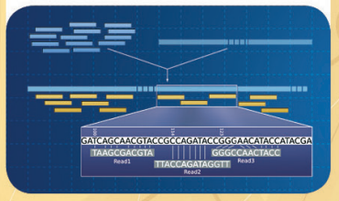


Integrated AI LLM Acceleration Solution

Modern LLMs(Large Language Models) require the extensive use of vector databases. MetisX AI Acceleration Solution supports integrating and expanding accelerators such as NPU to overcome the memory and data processing bottleneck in LLMs.

MetisX CXL Computational Memory Applications

NGS DNA Analysis

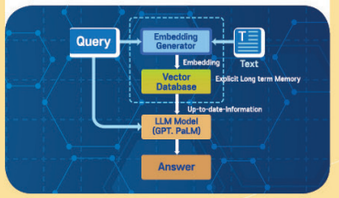


The current human DNA analysis based on CPU takes dozens of hours to align hundreds of GB of one person's data. MetisX Computational Memory completes DNA analysis in just a matter of minutes.

Data Analytics

Scale-out databases like Apache Spark are extensively utilized in ETL for data analytics. MetisX solution reduces the cluster size by offloading the analytics query engine to computational memory.

AI Vector Databases

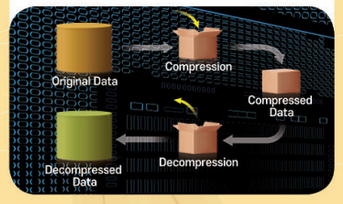


Recent LLMs utilize vector databases to retrieve updated information after training and to curb the rapid increase in model size. MetisX solution accelerates vector databases processing in memory, facilitating LLM advancement.

Graph Databases

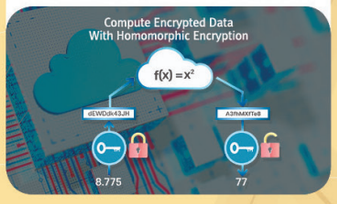
Graph databases, mainly utilizing pointer traversing, are extensively used in social media. Many cores with memory-optimized architecture of MetisX are suitable for accelerating graph processing efficiently.

Data Compression



Almost every data processing inevitably involves data compression. By offloading the compression to memory, it becomes possible to compress and decompress data faster and seamlessly than with the CPU or dedicated accelerators.

Homomorphic Encryption



Homomorphic encryption (HE) will be crucial in handling sensitive and essential data. SOTA algorithms are still slow on CPUs. Offloading HE algorithms into computational memory makes it possible to process data seamlessly.

MetisX Roadmap

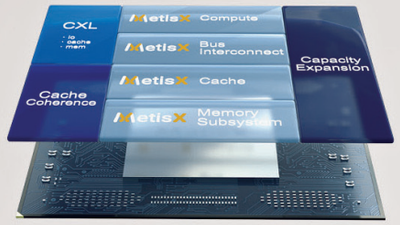
- **2022**
  - Founded
  - Seed Round KRW 8.5bn (USD 6.8mn) funded
- **2023**
  - NGS DNA Acceleration (FPGA)
  - Data Analytics Acceleration (FPGA)
- **2024**
  - CXL Petabytes-scale Infinite Memory (FPGA)
  - Series A Fund Raising
  - Vector DB Acceleration (FPGA)
- **2025**
  - CXL 3.0 Computational Memory ASIC
  - CXL 3.0 Computational Memory & Infinite Memory Customer Sample
- **2026**
  - Computational Memory Pool & Petabytes-scale Infinite Memory Pool
- **2027**
  - Next Generation CXL Computational Memory ASIC

Technologies

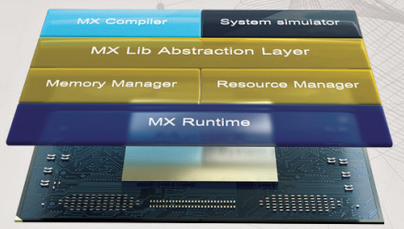
MetisX Data Domain-Specific Architecture

Highly Parallelized and Scalable Architecture for Large-Scale Data Processing
SW-Defined Acceleration Mechanism for Various Applications Offloading

- MetisX Vertically Optimized HW -



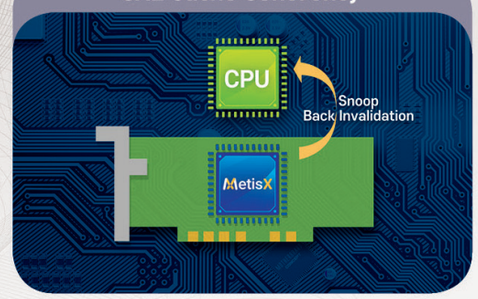
- MetisX SW Framework -



MetisX CXL Differentiations

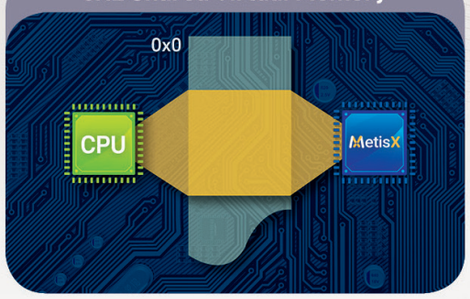
Differentiated CXL Technologies for MetisX Computational Memory

CXL Cache Coherency



Device Snoop Control Management
Simple Coherent Memory View

CXL Shared Virtual Memory



Device Address Translation
Flat Memory Model for Applications

MetisX Company Info

www.metisx.com
contact@metisx.com

Team

Memory Solution Experts with Data Domain Specific Architecture
Cutting-Edge Enterprise-Grade Semiconductor Experts with Experience in over 10+ ASICs
Strong HW and SW Teams for HW-SW Co-Architecting
SW-Defined Acceleration Mechanism for Various Applications Offloading

Funding

Successfully Completed KRW 8.5bn (USD 6.8mn) Seed Funding in Dec. 2022
Series A Round is Scheduled for the Mid of 2024